Amendments to the Specification:

Please amend the title as follows:

A1 "~~SPECULATIVE~~ REGISTER ADJUSTMENT BASED ON ADJUSTMENT VALUES DETERMINED AT MULTIPLE STAGES WITHIN A PIPELINE OF A PROCESSOR"

Please insert the following new paragraph after the paragraph beginning at page 3, line 16:

A2 FIG. 10 illustrates an example system.

Please replace the paragraph beginning at page 17, line 22 with the following amended paragraph:

A3 FIG. 8 illustrates a hybrid circuit having counters 110, 111, 114 in an AC stage and the first n - 1 execution stages. The circuit may allow the pipeline to execute its instructions following a termination if the termination occurs in an n^{th} execution stage or later. However, the circuit may adjust a speculative count register following a termination if the termination occurs in the $(n-1)^{th}$ execution stage or earlier. Again, the variable n may define the point at which allowing instructions to flow through the pipeline takes an amount of time less than or equal to the branch penalty. In other cases, the variable n may reside much earlier in the pipeline (e.g., where the branch penalty is larger). In still other cases, the variable n may be defined in terms of the number of stages rather than the number of execution stages.

Please replace the paragraph beginning at page 18, line 13 with the following amended paragraph:

A4

FIG. 9 illustrates an exemplary circuit for incrementing a speculative count register 150 in a hardware loop scenario. On each pass of loop, multiplexer 154 may decrement the speculative count register 150 using an adder 152. However, if adjustment is necessary (e.g. if a loop instruction is terminated before it commits), the adjustments signal 156 may adjust the speculative count register 150 accordingly. Once the loop has finished its last iteration, comparator 158 may send a signal 160 so indicating.

Please replace the paragraph beginning at page 18, line 23 with the following amended paragraph:

A5

Various embodiments of the invention have been described. For example, various techniques for adjusting a speculative register have been described for implementation within a processor. The processor may be implemented in a variety of systems including general purpose computing systems, digital processing systems, laptop computers, personal digital assistants (PDA's) and cellular phones. FIG. 10 illustrates an example system. In such a system, the processor 2 may be coupled to a memory device 8, such as a FLASH memory device or a static random access memory (SRAM) that stores an operating system and other software applications. These and other embodiments are within the scope of the following claims.